MEMPHIS: Holistic Lineage-based Reuse and Memory Management for Multi-backend ML Systems

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ABSTRACT

Modern machine learning (ML) systems leverage multiple backends, including CPUs, GPUs, and distributed execution platforms like Apache Spark or Ray. Depending on workload and cluster characteristics, these systems typically compile an ML pipeline into hybrid plans of in-memory CPU, GPU, and distributed operations. Prior work found that exploratory data science processes exhibit a high degree of redundancy, and accordingly applied tailor-made techniques for reusing intermediates in specific backend scenarios. However, achieving efficient holistic reuse in multi-backend ML systems remains a challenge due to its tight coupling with other aspects such as memory management, data exchange, and operator scheduling. In this paper, we introduce MEMPHIS, a principled framework for holistic, application-agnostic, multi-backend reuse and memory management. MEMPHIS's core component is a hierarchical lineage-based reuse cache, which acts as a unified abstraction and manages the reuse, recycling, exchange, and cache eviction across different backends. To address challenges of different backends such as lazy evaluation, asynchronous execution, memory allocation overheads, small available memory, and different interconnect bandwidths, we devise a suite of cache management policies. Moreover, we extend an optimizing ML system compiler by special operators for asynchronous exchange, workload-aware speculative cache management, and related operator ordering for concurrent execution. Our experiments across diverse ML tasks and pipelines show improvements up to 9.6x compared to state-of-the-art ML systems.

1 INTRODUCTION

Modern ML systems are widely used for model training, inference, as well as data preparation and feature transformations of multi-modal input data like text, images, and tabular data [100]. Data scientists hierarchically compose complex ML pipelines from black-box primitives [25]. The exploratory nature of these pipelines causes high computational redundancy [39, 66, 101, 125].

Sources of Redundancy: The high computational redundancy stems from various sources including incremental modifications of ML pipelines in AutoML and hyper-parameter tuning, as well as fine-grained redundancy in training, inference, and transfer learning [101]. AutoML and similar tools [37, 45, 78, 83, 114] combine tasks like data cleaning, feature engineering, hyper-parameter tuning, and model training [74, 75], and then explore various combinations with slight changes but, for instance, shared pre-processing. Deep neural network (DNN) workloads also execute data pipelines [53, 88, 92] and forward paths [93, 104] repeatably at a batch granularity. Similarly, inference frameworks for object detection and machine translation [30] encounter duplicate inputs [33, 73, 124].

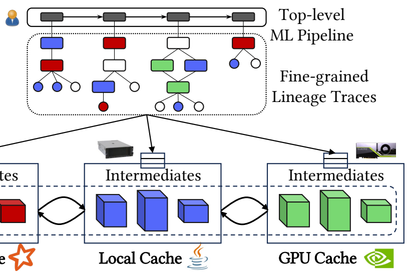


Figure 1: Multi-backend Reuse Cache for Intermediates.

Multi-backend ML Systems: ML pipelines with diverse data and workload characteristics necessitate multiple, specialized backends for achieving both efficiency and scalability, while utilizing available hardware resources and compute clusters. Example pipelines include (1) hybrid local/distributed runtime plans for large-scale ML [24, 85, 106, 129], (2) large-scale data validation [103, 109] and cleaning [114], (3) sampling, feature selection [25], and data augmentation [12, 34], which iteratively change data sizes by orders of magnitude, (4) exploratory ML algorithm research [86] (e.g., hybrid batch-minibatch training with large batch phases [15, 35]), (5) model training on datasets combining structured and unstructured features [93], (6) AutoML systems [24, 25, 78] supporting diverse ML algorithms, and (7) model debugging [80, 108] with configuration-dependent sizes of intermediates. These tasks are often combined into complex pipelines, increasingly fostering the development of ML systems with optimizing compilers, specialized operator placements [21, 25, 78], and multiple backends including local CPU/GPU/FPGAs, distributed MapReduce/Spark/Ray and federated backends [18, 69]. Example systems include PyTorch [96] and TensorFlow [2] (leverage CPU, GPU), MLlib [129] and Dask-ML [106] (utilize local and distributed), and SageMaker [78] (utilizes CPU, GPU, and Spark). Additionally, unified data analytics frameworks [21, 40, 49], polyglot [5, 47, 48], federated [18, 69], and composable [89] data management systems support cross-platform runtime backends.

Challenges in Multi-backend Reuse: Introducing a static reuse cache for redundancy elimination into multi-backend systems—as shown in Figure 1—poses major challenges due to heterogeneous backend characteristics. These backends differ in execution models (eager, lazy, asynchronous), memory characteristics (large distributed, small on-chip), data exchange bandwidths, other backend-specific properties like GPU memory allocation overhead, and target workloads, ranging from pre-processing to mini-batch DNNs. To address this diversity, modern ML systems employ various techniques for memory management [8, 61, 99, 126], operator placement [16, 17, 87], data exchange [53, 62, 92, 120, 132], and parallelization [44, 94, 113, 134] tailored to specific workloads and backends. This heterogeneity necessitates a principled approach for efficient reuse and robust cache integration across diverse compilation, memory management, and operator scheduling techniques, which is currently lacking.

Table 1: Prior Work on Reuse & Memory Management.

System	Reuse	Multi-backend	Mem.Mgmt.	Workload
HELIX [125]	Coarse	No	No	ML Pipelines
Clippr [33]	Coarse	No	No	Inference
LIMA [101]	Fine	No	No	All
MEMTUNE [126]	Fine	RDD	Yes	Spark Jobs
PyTorch [96]	No	Recycle GPU Ptr.	Yes	DNN
Capuchin [98]	No	Activations (GPU)	No	DNN
Cachew [53]	Coarse	Distributed	No	Preprocessing
VISTA [93]	Coarse	DNN Layers	No	Feature Extract
MEMPHIS	Fine	RDD, GPU Ptr.	Yes	All

Existing Work on Reuse: Prior work on reuse in ML pipelines rely on coarse-grained lineage tracing at the pipeline level to reuse coarse-grained results of the top-level primitives (see Figure 1) through compile-time materialization [39, 66, 116, 123, 125, 130]. However, this black-box view of individual preprocessing steps, feature engineering, and ML algorithms fails to handle the ubiquitous fine-grained redundancy (e.g., repeated matrix multiplications inside/across primitives) and non-determinism (randomized primitives). The LIMA framework [101] introduced fine-grained reuse, leveraging lineage traces on individual operations and functions to uniquely identify reusable intermediates, but was limited to local CPU operations. Table 1 summarizes the previous work, highlighting their reuse type, multi-backend reuse support, memory management capabilities (e.g. dynamic cache size), and target workloads. Prior work on application-specific, multi-backend reuse includes heuristics-based Spark RDD caching [10, 24, 53], input data pipeline reuse [53, 88, 92], prediction caching [33, 73], and GPU-CPU activation offloading for DNNs [58, 84, 98]. These approaches are tailored to specific workload-backend combinations, and fail to eliminate redundancy in modern data-centric ML pipelines with diverse tasks.

MEMPHIS Overview and Contributions: We introduce MEMPHIS, a holistic framework for efficient, multi-backend reuse of intermediates and memory management *inside* ML systems. Key principles are (1) a unified cache abstraction with system-internal API and multi-backend data objects, (2) backend-specific cache management, and (3) a robust integration with ML system compiler, runtime, and memory management, supporting diverse workloads. MEMPHIS is fully integrated into Apache SystemDS[1] [25], and utilizes *three* representative backends: SystemDS for in-memory operations, Spark for distributed operations, and GPUs for hardware acceleration. MEMPHIS extends LIMA's [101] lineage-based reuse framework—which eagerly caches all in-memory intermediates—with novel compiler and runtime techniques for reusing Spark and GPU intermediates, handling Spark's lazy evaluation and small GPU memory. Our detailed technical contributions are:

- *Background:* We discuss some background of ML-system internals, Spark, GPUs and their challenges in Section 2.
- *Hierarchical Lineage Cache:* Then in Section 3, we introduce our multi-backend lineage tracing framework and its unified tracing and reuse API for easier system integration.
- *Multi-backend Reuse:* We describe runtime cache management for Spark and GPU backends in Section 4, where we reuse Spark actions, RDDs, GPU pointers; their cache evictions; and combined reuse and recycling for GPUs.
- *Compiler Integration:* For holistic integration, we introduce novel compiler optimizations for workload- and reuse-aware speculative cache management (e.g. delayed caching, eviction injection), new asynchronous operators that enable overlapping computation with data transfer, and an operator ordering algorithm to maximize concurrent pipeline execution in Section 5.
- *Experiments:* Finally, we share results of several micro-benchmarks and diverse end-to-end workloads including data cleaning, model search, matrix factorization, inference, hyperparameter tuning, and transfer learning in Section 6. Compared to PyTorch and existing reuse frameworks, MEMPHIS yields substantial improvements.

2 BACKGROUND

This section describes the necessary background of ML system internals, Spark and GPU backends, their execution models, memory management, caching primitives, and challenges.

2.1 ML Systems Background

ML systems employ a range of compilation and execution strategies. Here, we focus primarily on SystemDS's program compilation, and multi-backend operator scheduling.

Program/DAG Compilation: We categorize the optimization scope of ML systems into three main types [26].

- *Eager Execution:* Libraries like NumPy [122], PyTorch [96], and Scikit-learn [97] execute the operations directly and rely on Python to handle control flow and variable scoping.
- *DAG Compilation:* Systems like TensorFlow [2, 20] perform lazy evaluation of a DAG of operations (i.e., larger scope of optimization) but rely on the host language (Python) for control flow interpretation. However, recent work like TF AutoGraph [90] and TorchDynamo [11] also extract and integrate control flow into the computation graph.
- *Program Compilation:* Julia [22] and SystemDS [25] (previously SystemML [24]) compile a script to a hierarchy of program blocks, with every last-level block is compiled into a DAG of operations. Similarly, Wayang [21] and Musketeer [49] compile scripts into cross-platform plans.

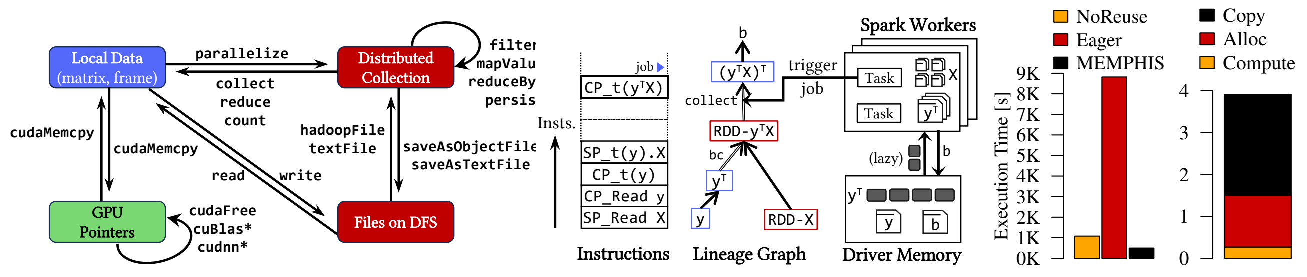
Compilation techniques like common subexpression elimination (CSE) and code motion fail to eliminate all redundancy, as the conditional control flow is often unknown during compilation.

Operator Scheduling: An operator scheduler converts operator DAGs into backend-specific instruction (kernel) streams and has two primary responsibilities: (1) *Operator placement* aims to minimize execution time of a multi-backend runtime and is done via global configurations, heuristics, or even reinforcement learning [87]. SystemDS places operations with higher memory estimates (than driver's memory) to Spark and compute-intensive, dense operations to GPU, both in a data locality-aware manner. Figure 2(a) shows the lifecycle of a data object in SystemDS across the host, Spark, and GPU, including backend-specific operations. (2) *Operator linearization* orders operator DAGs into instruction streams for sequential or parallel execution. The linearization

Table 2: Properties of Spark, GPU, and CPU.

	Exec.	Memory	Bandwd.	Cache-API	Workload
Spark	Lazy	Distrib.	15 GB/s	Yes	Large data
GPU	Async.	Small	6.1 GB/s	No	Mini-batch, DNN
CPU	Eager	Varying	—	No	ALL

[1]SystemDS: https://github.com/apache/systemds, and reproducibility package: https://github.com/damslab/reproducibility/tree/master/edbt2025-MEMPHIS



(a) Data Object Lifecycle (b) Spark Broadcast (c) RDD Reuse (d) GPU Timing

Figure 2: Spark and GPU Backend Details.

strategies affect parallelism and memory requirements. SystemDS linearizes DAGs to instruction streams in a depth-first manner and executes those on the respective backends.

Backends: The CPU, GPU, and Spark backends differ significantly in their execution model, memory management, and target workloads. Table 2 summarizes the key properties of Spark, GPUs, and CPUs, where the bandwidths are measured from the host (pageable host-to-device). Additional backends such as SystemDS federated [18, 19] or remote parfor [23, 24] create deeper hierarchies, where local lineage-based reuse directly apply.

2.2 Spark Backend and Challenges

Execution Model: Spark's execution model consists of a driver program for local operations and job scheduling, and multiple executor processes that run on worker nodes. RDDs (Resilient Distributed Datasets) [129] serve as a high-level programming abstraction, representing partitioned distributed collections of keyed matrix/frame tiles. Spark differentiates lazily evaluated *transformations* (distributed operations, which produce RDDs, see Figure 2(a)) and *actions*. An action (e.g. `count`, `collect`) triggers the `DAGScheduler` to construct and launch a Spark job. Each job is a DAG of stages, which comprise pipelined transformations separated by shuffle boundaries. The scheduler launches a task per partition, preferably in a data- or rack-local manner.

Memory Management: Spark's memory is divided into two regions: *execution* and *storage*. All Spark operations use the execution memory for computation and temporary partitions, while the storage is for caching and broadcasting. They share a unified memory (default 60% of heap) allowing execution to utilize unused storage memory and vice versa. There are two types of RDD caching. First, Spark implicitly caches shuffle files and broadcast data until destroyed. Caching shuffle files allows for avoiding recomputing the map side of a shuffle dependency [42]. Second, Spark provides the `persist()` API for explicitly caching RDDs (in different storage levels: deserialized/serialized and memory/disk) to avoid redundant lazy evaluation. The cached RDDs are lazily materialized in the executors' BlockManagers. Any subsequent job on a cached RDD then reads the partitions from memory or disk, thereby skipping prior operations. Spark evicts cached partitions if cached RDDs are too large or execution requires more memory. Evicted memory-only partitions or lost partitions on failures are recomputed based on Spark's lineage.

Broadcast: Broadcast-based operators like broadcast join are far less expensive than shuffle-based repartition joins. When a broadcast variable is created via `broadcast`, Spark creates a `TorrentBroadcast` that serializes and partitions the broadcast data into 4 MB chunks, and keeps them in the driver's `BlockManager` [43]. Individual chunks are then lazily transferred to selected executors, which parallelize the transfer to all executors on demand. Due to Spark's lazy evaluation, the broadcast data remains in the driver until the job completes.

Lazy Evaluation Challenges: Lazy evaluation presents several challenges for efficient reuse. First, traditional eager caching (e.g., LIMA, tf.Data [92], Cachew) eagerly materialize cached RDDs after each instruction, leading to performance drops due to repeated job executions. Figure 2(c) shows, eager materialization of 12K RDDs (4K reusable) is 10x slower than no caching at all. Second, runtime caching of all RDDs severely increases cluster memory usage (20x for experiments in Figure 2(c)), requiring speculative caching. Third, lazy evaluation delays the transfer of broadcast data to the cluster until the job execution triggers, requiring the retention of broadcast data and RDDs until the job completes. This creates *dangling references* that consume driver memory. For instance, Figure 2(b) shows linearized instructions (`SP` denotes Spark, `CP` denotes CPU) and the lineage graph for $b = (\mathbf{y}^\top \mathbf{X})^\top$, broadcasting $\mathbf{y}^\top$. The second transpose collects the vector $\mathbf{b}$ to the driver. The serialized $\mathbf{y}^\top$ remains in the driver's memory until the job finishes, which is dependent on other operators' linearization order. MEMPHIS employs workload-aware caching, lazy garbage collection and asynchronous job triggering, achieving a 2x speedup by reusing RDDs in Figure 2(c).

2.3 GPU Backend and Challenges

Execution Model: GPUs offer high peak performance and memory bandwidth, suitable for accelerating workloads with regular data access (e.g., DNN). SystemDS's GPU backend utilizes CUDA. Unlike Spark's lazy evaluation, CUDA kernel execution is eager and sequential within a single stream, but asynchronous for the calling host thread. Thus, the host thread continues executing other tasks while the kernels run concurrently. However, certain operations—such as device-to-host data transfer and memory deallocation—introduce synchronization barriers, which forces the CPU thread to wait until all pending GPU kernels have completed their execution. Traditional eager caching also forces synchronization barriers and slows down GPU execution.

Small Memory & Data Copy Challenges: To analyze GPU execution overhead, we ran an experiment with a single affine layer with ReLU activation for 10 epochs of 1K mini-batches of 128 rows. We force each kernel to allocate output memory, transfer the result to the host, and deallocate. Figure 2(d) shows that memory allocation/free and copy take 4.6x and 9x longer than the actual computation. This result highlights that static cache memory and traditional eviction policies, as seen in LIMA and Nectar [55], increase memory pressure and data copy overhead—making them unsuitable for GPU pointer caching. To mitigate these overheads, MEMPHIS employs dynamic cache sizes, memory recycling [132], and eviction injection optimizations.

3 HIERARCHICAL LINEAGE CACHE

The basic architecture of MEMPHIS with lineage tracing and a hierarchical cache—for seamlessly accommodating heterogeneous backends—is shown in Figure 3. The driver/host process handles the lineage tracing, compiler optimizations, and eviction planning, whereas the actual cached objects reside in the respective backends. This section describes our fine-grained lineage tracing, and the unified intermediate cache for backend-specific objects.

3.1 Supported API

MEMPHIS provides a set of system-internal methods to enable lineage-based reuse. This API simplifies the integration of MEMPHIS into any ML systems, irrespective of their backends and underlying compilation and operator placement strategies.

- `TRACE(inst)`: Trace lineage for an operator (Section 3.2).
- `SERIALIZE(trace)` / `DESERIALIZE(log)`: Serialize an in-memory lineage trace to a lineage log and vice versa.
- `RECOMPUTE(log)`: Recompute the exact same results from the provided lineage log. The execution environment for `RECOMPUTE` may differ from the original environment.
- `REUSE(trace)`: Reuse the instruction output if available in the cache and skip the instruction execution.
- `PUT(trace,object)`: Put the instruction result in the cache with backend-specific pointers.
- `MAKE_SPACE(object)`: Iteratively evict cached objects to make space for a new object in the corresponding backend.

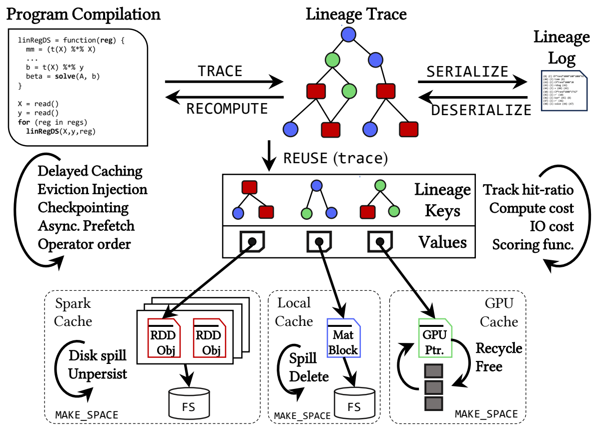
Improvements over LIMA: MEMPHIS builds upon LIMA's [101] basic lineage tracing (eager caching), and extends it with a hierarchical lineage cache and unified API for reuse across local, Spark, and GPU, robustness optimizations, and a holistic integration with ML systems. LIMA benefits moderate workloads, while MEMPHIS tackles complex multi-backend ML pipelines.

3.2 Backend-agnostic Lineage Tracing

A lineage trace—incrementally built at runtime—is a DAG with nodes and edges representing operations and data dependencies.

Fine-grained Lineage Tracing: We call `TRACE` for each linear algebra instruction before its execution (see pseudo-code in Figure 4). MEMPHIS internally maintains a hash map (`LineageMap`) to map the live variable names to the respective lineage DAGs. A lineage item contains the opcode, data items, and pointers to the input lineage items. During tracing, each output generates a new lineage item from input items, which is then added to the `LineageMap`. For efficient lineage DAG comparisons (probing), which is a core operation for reuse, lineage items implement `hashCode` and `equals`. We calculate the hash by hashing the hashes of the input items, the opcode, and the data items. For equality check, we rely on a non-recursive, queue-based approach with sub-DAG memoization and early abort conditions based on hash mismatches, height differences, and shared sub-DAGs (object identity). This simple yet scalable backend-agnostic lineage tracing is a solid foundation for additional backends.

Recomputation for Debugging: To tackle interpretability and debuggability of complex ML tasks involving heterogeneous backends, we enable easy sharing of serialized lineage traces and exact recomputation of intermediates. The `RECOMPUTE` API first deserializes a lineage trace into an in-memory lineage DAG, followed by applying the full compilation chain to generate the instructions. Full re-compilation ensures the same results and flexibility regarding configurations and hardware environments.


```
linRegDS = function(reg) {
  mm = (t(X) %*% X)
  ...
  b = t(X) %*% y
  beta = solve(A, b)
}

X = read()
y = read()
for (reg in regs)
  linRegDS(X,y,reg)
```

Figure 3: Hierarchical Lineage Cache & Reuse Overview.

Future work includes query processing on lineage traces for model management [117].

3.3 Multi-backend Lineage Cache

We leverage the property that the lineage uniquely identifies an intermediate for reusing previously computed intermediates. Our lineage cache serves as a repository for these lineage traces, maintaining the necessary data structures to efficiently map them to their corresponding backend-specific data objects.

Lineage Cache: The lineage cache is a hash map that maps lineage items to cached data objects (see Figure 3 middle). Figure 4 shows the pseudo-code of the reuse logic integrated in the main instruction execution path, which seamlessly applies to all instructions. We call `REUSE` for each instruction. If the output exists in the cache, we reuse the data object, assign it to the live variable, and skip the instruction. Otherwise, we execute the instruction and store the output in the cache via `PUT`. Additionally, the lineage cache entries hold metadata including compute costs, access counts, and status.

```
while (inst in insts)
  lt = TRACE (inst)
  if (!REUSE (lt))
    out = exec(inst)
    PUT (lt, out)
```

Figure 4: Reuse API.

Redundancy in Lineage Items: Generating a new lineage item object for each instruction *before* reuse creates redundant lineage DAGs across `LineageMap` and lineage cache entries. To address this, upon successful probes, we replace the respective `LineageMap` entries with the lineage keys of cached objects. As Figure 5 shows, this compaction increases shared sub-DAGs (objects with identical references), which in turn improves probing efficiency and reduces the memory footprint.

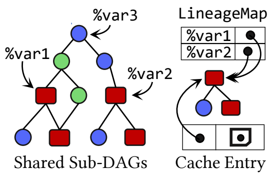


Figure 5: Compaction.

Backend-local Cached Objects: The lineage cache entries are wrappers around backend-specific pointers. These pointers refer to in-memory matrix blocks, scalars, distributed RDDs, GPU objects, and disk-evicted binaries. This design allows seamless data movement like broadcasting local inputs to remote backends, transferring Spark job results to the driver, and GPU-to-host copies. Moreover, the wrappers enable caching the same object in multiple backends, which is beneficial for data-local scheduling. The centralized lineage tracing and reuse facilitates a reuse-aware compilation to increase reuse potentials and reduce caching overheads. Figure 3 summarizes the lineage tracing lifecycle, reuse operations, backend-local evictions, and compiler extensions.

Multi-level Reuse: MEMPHIS reuses outputs of deterministic functions and basic blocks (code block w/o control flow) when called repeatedly with the same inputs, even when the inputs and outputs are scattered across different backends. We use a special lineage item containing the function name and inputs for each function output [101]. These items are managed alongside regular entries and are subject to eviction by the respective backends. Combining coarse-grained reuse (e.g., function reuse) with fine-grained reuse (e.g., operator-at-a-time reuse, as shown in Figure 4) is advantageous for hierarchically-composed data-centric ML pipelines. Multi-level reuse effectively reduces fine-grained remote operations, related data exchange, and cache pollution (avoids caching large distributed objects, or many small GPU objects) and hence is resilient against cache evictions.

4 RUNTIME MULTI-BACKEND REUSE

The backend-local caches require tailor-made cache management strategies due to their diversity. In this section, we describe the reuse and memory management for Spark and GPU.

4.1 Reuse and Memory Management in Spark

We utilize Spark's caching API to cache RDDs in Spark cluster memory. Furthermore, we introduce memory management and cache eviction techniques tailored for Spark's lazy evaluation.

Reuse Spark Actions: Spark actions trigger job execution and return the results to the driver. ML systems implicitly leverage these actions within distributed physical operators (e.g., single-block aggregates calling `reduce()` instead of `reduceByKey()`). Additionally, operator placement decisions may explicitly move data to the driver using `collect()`. Before triggering a Spark job, we reuse the previously collected result if available in the driver's cache, and bypass the job execution. In Figure 6 (top entry), the `transpose` operator collects the vector **b** to the driver and stores it in the cache for future reuse. Reusing redundant actions in the driver eliminates distributed operations, unnecessary distributed caching, and data exchange such as shuffle and collect.

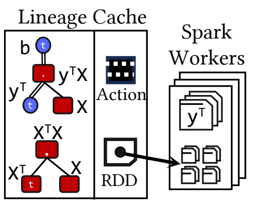


Figure 6: Spark Reuse.

Reuse RDDs: RDDs are distributed data collections, which are cached and reused in the cluster. Before executing a Spark transformation, the `REUSE` API probes the lineage cache and reuses the RDD (serves as a pointer to the distributed collection) if a match is found. Otherwise, we mark the RDD for caching with `persist()` and store it in the cache along with related metadata. `persist` is a lazy operation—and thus, the cached RDD may not be materialized in Spark memory by the time of reuse. However, we reuse even unmaterialized RDDs to enhance compute-sharing across jobs, and enable shuffle-file reuse (data exchange optimization). Figure 6 (bottom entry) shows a cached RDD entry for $\mathbf{X}^\top\mathbf{X}$, where $\mathbf{X}$ is distributed.

Lazy Garbage Collection: To tackle memory overhead caused by dangling RDDs and broadcast references (see Figure 2(b)), we track internal metadata for each RDD, including #child RDDs, #pending consumers, materialization status, and its memory overhead. During reuse, the `MAKE_SPACE` function recursively traverses child RDDs and broadcasts, updating the metadata and cleaning up stale RDDs (not in use and already materialized). For example, in Figure 6 (bottom), we clean up $\mathbf{X}^\top$ and $\mathbf{X}$ once $\mathbf{X}^\top\mathbf{X}$ is materialized. We use Spark's `destroy` and `getRDDStorageInfo` methods for broadcast variable deletion and materialization checks. Furthermore, to mitigate caching overhead, the MEMPHIS compiler often defers RDD caching (*delayed caching* discussed in 5.2). Delayed caching along with Spark action reuse further increases dangling references. In Figure 6 (top), $\mathbf{y}^\top\mathbf{X}$ RDD caching is delayed and remains unmaterialized due to the reuse of the collected **b** at the driver. Such RDDs prevent the garbage collection of their child RDDs (i.e., $\mathbf{y}^\top$, $\mathbf{X}$). After k cache misses, we asynchronously trigger a Spark job (calling `count()`) to materialize such an RDD. Any subsequent reuse then cleans up the child RDDs. These lazy cleanups ensure periodic reclamation of driver and cluster memory without hindering reuse.

Cache Eviction: We employ a cost-based eviction policy (orthogonal to Spark's partition-level eviction) to remove RDDs (via `unpersist`) with low reuse potential, preventing Out-of-Memory (OOM) errors. We heuristically utilize 80% (configurable) of Spark's storage memory for reuse, and the rest for broadcast variables and compiler-placed checkpoints (discussed in Section 5.2). We extend the prior Cost&Size policy [39, 101], which aims to preserve objects with high compute-cost-to-memory ratios, for Spark's lazy evaluation. In detail, we rank the operators based on analytical compute cost $c(o)$, and we collect statistics for each cached RDD o including the estimated worst-case size $s(o)$ and the number of references (#hits: r_h, #misses: r_m, #jobs: r_j), which are updated during every reuse and account for global reuse potential. The eviction scoring function for o is

$$\arg\min_{o \in \mathrm{Q}} \quad (r_h(o) + r_m(o) + r_j(o)) \cdot c(o)/s(o) \tag{1}$$

where Q is the priority queue of RDDs. The `MAKE_SPACE` method marks RDDs for eviction via `unpersist` and refreshes cache metadata (e.g., available memory) with actual values (using `getRDDStorageInfo`). `unpersist` is an asynchronous operation, causing temporary overflow of the storage region, which is handled by Spark's partition spilling with minimum overhead. This eviction policy, combined with Spark's partition spilling, performs well in a wide variety of use cases.

Example 4.1 (Grid Search Linear Regression). In this example, we apply grid search hyper-parameter tuning on a direct-solve linear regression (`linRegDS`) for feature matrix **X** (distributed) and responses **y** (local). Figure 7 (comprising Figures 2(b) and 6) shows the `linRegDS` function, which is called by grid search for a list of regularization parameters (`reg`). The core operations $\mathbf{X}^\top\mathbf{X}$ and $\mathbf{X}^\top\mathbf{y}$ are independent of `reg` and thus, reusable across `linRegDS` calls. SystemDS compiles a shuffle-based matrix multiplication for $\mathbf{X}^\top\mathbf{X}$ and a broadcast-based multiplication for $\mathbf{X}^\top\mathbf{y}$ after rewriting it to $(\mathbf{y}^\top\mathbf{X})^\top$ (broadcasting $\mathbf{y}^\top$). The second transpose of $(\mathbf{y}^\top\mathbf{X})^\top$ and the `solve` trigger Spark jobs. Figure 7 shows

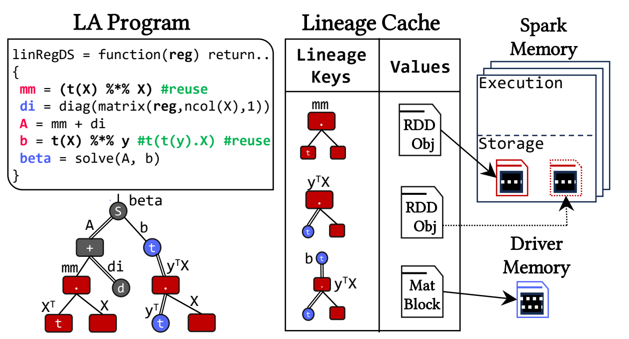

```
linRegDS = function(reg) return..
{
 mm = (t(X) %*% X) #reuse
 di = diag(matrix(reg,ncol(X),1))
 A = mm + di
 b = t(X) %*% y #t(t(y).X) #reuse
 beta = solve(A, b)
}
```

Figure 7: Spark Action and RDD Reuse Example.

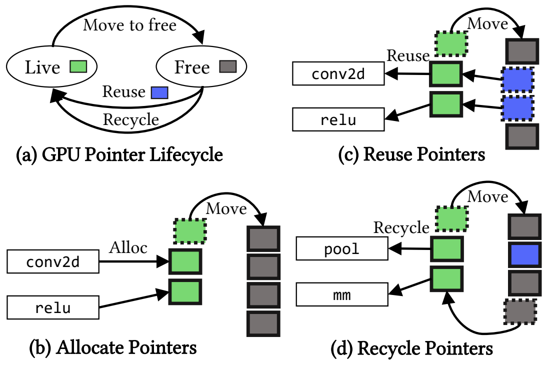


Figure 8: Reusing and Recycling of GPU Pointers.

the DAG for `linRegDS`. Rectangles represent distributed operations. Reusable distributed and local operations are colored red and blue, and data exchange is indicated by double lines. The first `linRegDS` call creates lineage cache entries for all operations and caches in-memory matrix outputs of local operations. The second transpose of $(\mathbf{y}^\top \mathbf{X})^\top$ caches the collected column vector **b** as an in-memory matrix in the driver. Our compiler enables delayed caching for RDDs, e.g., deferring caching until the second cache hit. Accordingly, the second `linRegDS` call marks the RDDs (**mm**, $\mathbf{y}^\top\mathbf{X}$) for distributed caching, reuses the local operations and the collected **b**. Reusing the Spark action result **b** entirely eliminates the need to trigger the Spark job. However, not triggering the job keeps $\mathbf{y}^\top\mathbf{X}$ RDD unmaterialized in the executors. The third call reuses the **mm** RDD, and subsequent calls clean up its child RDDs. After k (default three) cache misses for $\mathbf{y}^\top\mathbf{X}$ RDD, we asynchronously materialize the $\mathbf{y}^\top\mathbf{X}$ RDD (dotted line).

4.2 Reuse and Memory Management in GPU

To manage GPU's small memory and allocation overhead, we combine reuse and recycling in a unified memory manager with moving boundaries, where we reuse `pointers` to previous results. Figure 8 depicts the memory management operations.

Live Variable Management: All pointers from allocation to deallocation are managed by the lineage cache. Figure 8(a) shows the lifecycle of a GPU pointer. We organize the allocated pointers in two lists: a `Live` and a `Free` list. The `Live` pointers correspond to variables which are still in use (i.e., pending consumers). The `Free` list comprises a hash map that maps sizes to a priority queues of free pointers of the respective sizes. Before executing an operation, we allocate memory for the output via `cudaMalloc` and place the allocated pointer in the `Live` list. After the last use, the pointers are moved to the `Free` list, as shown in Figure 8(b). This strategy of maintaining free memory pools benefits mini-batch processing with fixed batch sizes.

Reuse: Lineage cache entries encapsulate GPU pointers and related metadata like data characteristics. Before executing an instruction (composed of one or more GPU kernels), the `REUSE` call reuses the output pointer if available in the cache and skips launching the kernels. As Figure 8(c) shows, `REUSE` moves the reused pointer from `Free` to `Live` list. Reusing a pointer multiple times leads to multiple variables referencing a single pointer. We track the *reference count* for each pointer indicating the number of live variables referencing it, and only when the reference count becomes zero, the pointer is returned to the `Free` list.

Memory Recycling: All pointers in the `Free` queues are subject to eviction (preventing OOM). Pointers in each queue are ordered according to a scoring function. Algorithm 1 shows the

Algorithm 1 Allocate memory of size s

```
Input: Size $s$, Size-specific free pointer lists $FL$
Output: Allocated memory pointer A
 1: if CANALLOCATE(s) then                                   // GPU is not full
 2:     A = CUDAMALLOC($s$)                                  // Allocate new memory
 3: else if $FL$.CONTAINS($s$) then                          // Find free pointer of size s
 4:     A = $FL$.GETFREEPOINTEREXACT($s$)                    // Recycle
 5: else if $s \le FL$.LARGEST() then                       // Find pointer of size > s
 6:     $tmp = FL$.GETFREEPOINTERLARGERTHAN($s$)
 7:     CUDAFREE($tmp$)                                      // Deallocate
 8:     A = CUDAMALLOC($s$)                                  // Allocate new memory
 9: else if $s > FL$.LARGEST() then                         // s > all free pointers
10:     $freedSize = 0$                                      // Repeatedly deallocate
11:     while $freedSize < s$ | A is NULL do
12:         $tmp = FL$.GETFREEPOINTERNOTEXACT($s - freedSize$)
13:         $freedSize = freedSize + tmp$.SIZE()
14:         CUDAFREE($tmp$)
15:         if $freedSize \ge s$ then
16:             A = CUDAMALLOC($s$)                          // Allocate new memory
17: if A is NULL then
18:     $FL$.CLEARALL()                                      // Clear all free pointers
19:     A = CUDAMALLOC($s$)                                  // Allocate new memory
```

details for serving an allocation request. Once the GPU memory is full, as shown in Figure 8(d), we start recycling the free pointers as a form of eviction. We first look for a free pointer with the exact size to recycle. If not available, we free a pointer just larger than the required size using `cudaFree` (which may cause fragmentation). If all free pointers are smaller than the required size, we repeatedly free a pointer until `cudaMalloc` is successful. If these steps fail, we clean up all free pointers. Even then, the allocation may fail due to many live variables and memory fragmentation. In such cases, we initiate the device-to-host eviction process (not shown in Algorithm 1), and finally a full defragmentation—though this is rare in practice. Memory recycling benefits typical DNN workloads with repeated operations on fixed-sized intermediates, such as the forward and backward passes of mini-batch processing. We prioritize recycling exact-sized memory chunks over temperature-based approaches to prevent GPU memory fragmentation and to avoid the costly defragmentation process. The primary objective of these steps is to avoid memory allocation, deallocation, which triggers device synchronization, and fragmentation due to repeated deallocation, however, without compromising the reuse potential.

Eviction Policy: The eviction policy determines the order in which pointers are recycled or freed from each free queue. Our policy is devised to serve typical mini-batch workloads. The eviction scoring function for a cached GPU object o is

$$\arg\min_{o \in \mathrm{Q}} \quad T_a(o) + 1/h(o) + c(o) \tag{2}$$

where Q is a priority queue of free pointers. $T_a(o)$ denotes the normalized last access timestamp, preserving recently reused pointers from recycling (e.g. reuse within a mini-batch). $h(o)$ denotes the height of the corresponding lineage trace. The $1/h(o)$ factor preserves objects with shorter lineage traces, allowing reuse of *input data pipelines* [88] that are applied to mini-batches, where a mini-batch is sliced from the input datasets before starting the forward pass. The lineage DAGs for operations in these data pipelines are shorter since they are directly sliced from the input (compared to the operations in forward/backward paths). Finally, $c(o)$ is the estimated compute cost of object o, which enables recycling the least expensive intermediates first (e.g., element-wise `ReLU` before `Conv2d` or fully-connected layers).

5 COMPILER INTEGRATION

Runtime-level reuse and memory management are valuable, but a holistic handling at *compiler- and runtime-level* yields additional improvements. In this section, we describe optimizations for operator parallelism, data exchange, workload-aware cache management and checkpoint placement, as well as an operator linearization strategy to increase parallel execution.

5.1 Asynchronous Remote Jobs

To enable inter-backend parallelism and asynchronous data transfer, we introduce new operators and related rewrites.

Prefetching Remote Objects: We introduce a new `prefetch` operator and the corresponding compiler rewrite to trigger remote (Spark/GPU) jobs and asynchronously fetch the results without blocking the CPU instruction stream. This rewrite traverses the execution plan and identifies operators that trigger remote jobs through `collect` and `cudaMemcpyDeviceToHost` calls. These operators represent the roots of remote operator chains. After each such root, the rewrite inserts a `prefetch` instruction, wrapping the triggering call, and marks it for asynchronous execution. Additionally, this rewrite flags all other Spark actions for asynchronous execution. At runtime, the operator scheduler triggers these asynchronous operations and returns `future` objects [91], allowing concurrent execution. This compiler extension enables concurrent execution of Spark jobs, local operators, and GPU kernels. Figure 9(a) shows the DAG from Example 4.1 (Figure 7) after `prefetch` placement (indicated by *pf*) for two jobs that collects results of **mm** + **di** and $\mathbf{y}^\top\mathbf{X}$, respectively.

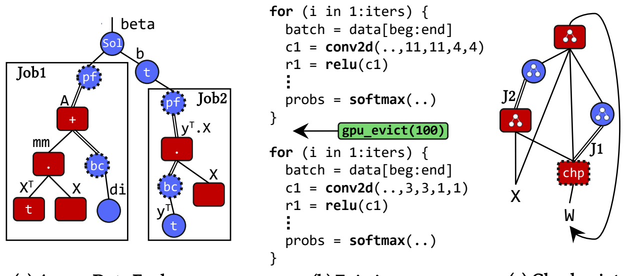
Reusing Prefetched Results: Caching results immediately after instruction execution is infeasible for asynchronous operators. To overcome, the main thread propagates the corresponding lineage trace to the spawned prefetch threads, enabling them to cache (`PUT`) the fetched data once available. The `prefetch` instruction of Job2 in Figure 9(a) caches the fetched result of $\mathbf{y}^\top\mathbf{X}$, which is then reused (e.g., in `prefetch`) in subsequent iterations.

Broadcasting Local Objects: We introduce another asynchronous operator, `broadcast`, to optimize local to remote data transfer. The corresponding rewrite places broadcast as the last operator of local operator chains. For Spark, the broadcast operator asynchronously partitions the input matrix and registers it as a broadcast variable, deferring the actual data transfer to the executors until the broadcast variable is used by Spark. Figure 9(a) shows an example of broadcast instruction (*bc*) placement.

5.2 Workload-aware Cache Management

We introduce new operators for cache management and rewrites for their placements. These operators aim to reduce caching overhead and improve the utility of reuse and memory management.

Eviction Injection: Our eviction logic, (in Section 4), operates in an incremental manner, evicting one object-at-a-time to make space for new objects. This approach incurs high eviction overhead during allocation pattern shifts, common in GPU workloads. Figure 9(b), shows an ensemble learning script that utilizes two pre-trained models (AlexNet & VGG16) for joint prediction. In the first `for` loop, MEMPHIS efficiently recycles the less reusable pre-allocated pointers. However, the allocation pattern shifts in the second loop due to varying `conv2d` kernel sizes, leading to high allocation-deallocation overhead and memory fragmentation. To mitigate this issue, we introduce the `evict` instruction for cache cleanup. A program-level rewrite identifies these loop patterns and injects `evict` instructions with percentages of cache



```
for (i in 1:iters) {
  batch = data[beg:end]
  c1 = conv2d(..,11,11,4,4)
  r1 = relu(c1)
  ⋮
  probs = softmax(..)
}
for (i in 1:iters) {
  batch = data[beg:end]
  c1 = conv2d(..,3,3,1,1)
  r1 = relu(c1)
  ⋮
  probs = softmax(..)
}
```

(a) Async. Data Exchange (b) Eviction (c) Checkpoint

Figure 9: Compiler-assisted Reuse (incl. Asynchronous Data Exchange and Operations, Forced Eviction, and Checkpointing).

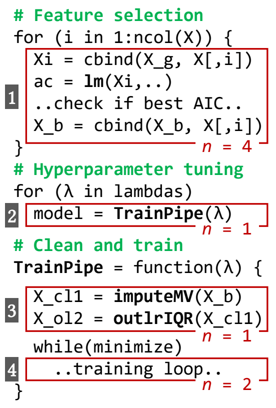
size to clean up as arguments. At runtime, the `evict` instruction utilizes the backend-specific eviction logic to free up space. The rewrite avoids full eviction if access patterns repeat. Other DNN frameworks require manual placement of such cleanup [31].

RDD Checkpoint Placement: Lineage-based reuse eliminates redundancy across Spark jobs, but Spark's lazy evaluation introduces another form of redundancy due to shared dataflow dependencies between jobs. Prior work [10, 24] proposes simple, rule-based checkpoint (`persist`) placements. In this work, we introduce two workload-aware compiler rewrites for checkpoint placement. (1) The first rewrite identifies overlapping Spark jobs within a basic block and injects a checkpoint after the last shared operator. (2) The second rewrite targets common iterative algorithms, where updated variables create increasingly large operator graphs. Figure 9(c) shows a simplified DAG of one factor matrix **W** of Poisson Non-negative Matrix Factorization [79]. Here, each node represents a Spark (red) or local (blue) operator chain. Every iteration updates **W** and triggers two jobs (J1, J2), both lazily executing all previous iterations. Our rewrite identifies the variables that are updated in each iteration and places checkpoints to reuse previous iterations' results. In this example, we cache **W** (indicated by *chp*) in each iteration. For a seamless integration, at runtime, the lineage cache eviction tracks these checkpointed RDDs and updates the cache metadata.

Delayed Caching: Caching incurs a probing cost and other backend-specific overheads, especially for long-running, complex workloads. Caching non-repeating large RDDs increases memory pressure and garbage collection overhead on both executors and drivers. Similarly, DNN training with no reuse potential in GPUs suffer from allocation overhead, memory fill-up, and fragmentation. Empirically, reusable operations repeat multiple times for hierarchically composed ML pipelines. Based on this observation, we introduce *delayed caching*, that defers caching until the n-th (*delay factor*) cache hit. At runtime, the `PUT` call creates an empty lineage cache entry with status `TO-BE-CACHED` upon the first cache hit. If the operator repeats n times, we put the actual object in the cache and change the status to `CACHED`. Together with our cache eviction schemes, cache entry strategies such as delayed caching substantially reduce the overhead and cache misses.

Automatic Parameter Tuning: We introduce a program-level rewrite for tuning the *delay factor* n (no delay is n = 1) and the *Spark storage level* (for RDD caching) of each basic block, based on estimated reuse potential. This rewrite recursively traverses all program blocks, analyzing the execution frequency (nested loops, function calls) and the presence of loop-dependent operations (not reusable). A second pass then assigns the values for n (n = 1 if >80% reusable) and storage level, and stores them in the block headers.

Figure 10 shows a *simplified* ML pipeline where, operations in block 1 (step-wise feature selection [3]) are loop-iteration-dependent ($\mathbf{X}_i$ varies with i) and thus, is deemed not reusable ($n = 4$). In block 3, cleaning and outlier removal methods `imputeMV` and `outlrIQR` are independent of λ and thus, reusable ($n = 1$). The training in block 4 is partially λ-dependent ($n = 2$). Similarly, we assign storage level `MEMORY_AND_DISK` to block 2 and 3, and `MEMORY` (avoids spilling to disk) to 1 and 4, respectively.



```
# Feature selection
for (i in 1:ncol(X)) {
  Xi = cbind(X_g, X[,i])
  ac = lm(Xi,..)
  ..check if best AIC..
  X_b = cbind(X_b, X[,i])
}                          n = 4
# Hyperparameter tuning
for (λ in lambdas)
  model = TrainPipe(λ)
                           n = 1
# Clean and train
TrainPipe = function(λ) {
  X_cl1 = imputeMV(X_b)
  X_ol2 = outlrIQR(X_cl1)
                           n = 1
  while(minimize)
    ..training loop..
}                          n = 2
```

Figure 10: Delay Factors.

5.3 Operator Ordering

Traditional backend-agnostic operator ordering is suboptimal for multi-backend systems. For a holistic inter-backend parallelism via asynchronous operators, we introduce a new operator ordering algorithm, MAXPARALLELIZE that aims to maximize opportunities for concurrent execution of local and remote operator pipelines. As Algorithm 2 shows, we identify the operator chain roots (Spark action/prefetch/GPU-to-host copy) and linearize them in descending order of their lengths to maximize parallelism—longer operator chains allow for more concurrent execution, thus increasing the degree of parallelism. The DEPTHFIRST method recursively processes sub-DAGs, with node memoization. This tight operator packing also improves memory usage by reducing the lifetime of dangling RDD references [70]. For Figure 9(a), MAXPARALLELIZE linearizes Job1 followed by Job2. The `prefetch` operators trigger these jobs concurrently, where `solve` and transpose wait on the `future` objects for results.

5.4 Applicability and Design Decisions

Our reuse and cache management for Spark apply to other distributed backends with lazy evaluation that offer primitives for distributed caching. For instance, Dask [106] and Ray [91] provide `Cache` [38] and `Checkpoint` [102] interfaces, respectively. Similarly, our memory management and reuse for GPU can be extended to other hardware accelerators like FPGAs and TPUs [64]. Here, we summarize the applicability and future work.

- *Other ML Systems:* MEMPHIS applies to other compilation-based, multi-backend systems for unified data processing [21, 49], integrated data analysis [36], polyglot, and AutoML. Our compiler and runtime optimizations like RDD reuse, cleanup, and eviction and checkpoint injection also apply to DAG compilation in TensorFlow and PyTorch.
- *Multi-GPU/stream:* SystemDS does not support multi-GPUs/GPU-streams. However, the memory manager and *prefetch* logic apply to multiple GPUs with separate caches.
- *Deeper Hierarchies:* For hierarchically-structured backends (e.g. federated workers with local GPUs), local lineage-based reuse directly applies. Prior work added lineage-based reuse to multi-tenant federated workers [19]. Future work includes efficient transfer of lineage traces.
- *No Exchange of Cached Objects:* While we implemented the mechanics for evicting cached objects from one backend to another, we observed that moving cached objects cause movements of live variables for maintaining data locality, which in turn can severely affect overall execution time.
- *Operator Scheduling:* Our scheduling strategies provide holistic memory management, but in a heuristic manner. Devising a guaranteed optimal, cost-based and reuse-aware operator placement is interesting future work.

Algorithm 2 Operator linearization

```
Input: Operator DAG $D$ with root $R$
Output: List of instructions $\mathbf{L}$
 1: if HASNOREMOTEOPS(D) then                              // All local OPs
 2:     $\mathbf{L}$ = DEPTHFIRST($D$)                          // Linearize deapth-frist
    // Step1: Identify OP chains & count operators
 3: $SRoots$ = COLLECTSPROOTS($D$)                           // Identify Spark jobs
 4: $GRoots$ = COLLECTGPROOTS($D$)                       // Identify GPU OP chains
 5: for each list $Roots$ in $SRoots, GRoots$ do
 6:     for each root $r$ in $Roots$ do
 7:         if $r$ is Spark then
 8:             $nSPOps[r]$ = COUNTSPOPS($r$)             // Spark OP count/job
 9:         else if $r$ is GPU then
10:             $nGPOps[r]$ = COUNTGPOPS($r$)        // GPU OP count/chain
    // Step2: Sort and linearize remote jobs (longer jobs first)
11: $Roots = SRoots + GRoots$
12: $Roots$ = SORTROOTSBYOPCOUNT($SRoots, nSPOps, nGPOps$)
13: for each root $r$ in $Roots$ do
14:     if $r$ is Spark then
15:         DEPTHFIRST($r, nSPOps[r], \mathbf{L}$)          // Depth-first Spark jobs
16:     else if $r$ is GPU then
17:         DEPTHFIRST($r, nGPOps[r], \mathbf{L}$) // Depth-first GPU OP chains
    // Step3: Linearize the rest of the local OPs
18: DEPTHFIRST($R, \mathbf{L}$)                          // Place unvisited nodes of D
```

6 EXPERIMENTS

Our experiments study MEMPHIS's performance by systematically scaling data sizes, task complexity, and instruction counts across various workloads. We first conduct micro benchmarks for understanding the overhead of lineage tracing and cache probing in Spark and GPUs. Subsequently, we investigate a range of end-to-end ML pipelines, including data pre-processing, hyper-parameter optimization, matrix factorization, and DNN, for exploring the benefits of multi-backend reuse in realistic settings.

6.1 Experimental Setting

HW Environment: We ran all experiments on a cluster of 8+1 scale-out nodes and a single scale-up node. Each scale-out node has an AMD EPYC 7443P CPU @ 2.8-4.0 GHz (24 physical/48 virtual cores), and 256 GB DDR4 RAM. The scale-up node has two Intel Xeon Gold 6338 CPUs @ 2.2-3.2 GHz (64 physical/128 virtual cores), 1 TB DDR4 RAM, and two NVIDIA A40 GPUs with 48 GB and PCIe 4.0. The software stack comprises Ubuntu 20.04.6, Hadoop 3.3, Spark 3.5, OpenJDK 11, CUDA 10.2, and CUDNN 7.6.

Memory Configurations: For the Spark cluster, we use 38 GB driver memory and 230 GB executor memory. The buffer pool and operation memory are set to 20 GB and 7 GB i.e., operators requiring more than 7 GB memory are compiled to Spark instructions. The lineage cache size is set to 5 GB on the driver and 55 GB (80% of storage) on each executor. The scale-up node has 200 GB heap with 10 GB host memory for lineage cache and the full 48 GB GPU memory for the unified memory manager.

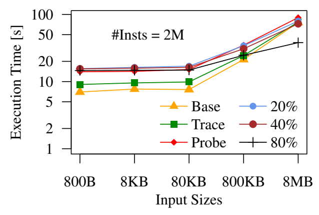
Baselines: For a comprehensive evaluation, we compare MEMPHIS with different SystemDS configurations, application-specific reuse frameworks, and state-of-the-art ML systems.

- *SystemDS:* **Base** is SystemDS without reuse. **MPH** denotes MEMPHIS with multi-level, multi-backend reuse and all optimizations. Different configurations of SystemDS (**Base-x**) and MEMPHIS (**MPH-x**) are introduced later.
- *Reuse Frameworks:* We compare with several reuse frameworks: LIMA [101] for fine-grained reuse, HELIX [125] for coarse-grained reuse, CoorDL [88] for *input data pipeline* reuse in CPU, Clipper [33] for prediction reuse, and VISTA [93] for reuse in transfer learning. For fair comparisons, we hand-optimized the ML pipelines via script-level common subexpression elimination (CSE) to reuse outputs of built-in functions (which may contain multi-backend operations), as well as data pipeline results, predictions, and extracted features for transfer learning, mimicking the capabilities of these frameworks. Script-level reuse ensures the maximum possible reuse benefits without overheads and configuration complexities from these frameworks.
- *ML System:* We compare with PyTorch 2.1 [96], a strong baseline for DNN workloads on GPUs. PyTorch's caching memory allocator also recycles memory blocks [31, 76].

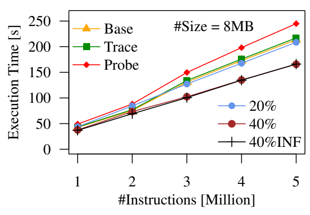
6.2 Micro Benchmarks

We first conduct micro benchmarks to study various aspects of MEMPHIS in isolation. We use representative but simplified scripts. These experiments focus on lineage tracing and reuse overhead, cache size configuration, and memory management of Spark and GPU. For the micro benchmarks, we set SystemDS's buffer pool to 100GB while keeping the operation memory constant at 7GB to prevent buffer pool eviction. While evaluating the impact of varying cache sizes in the driver, we keep remote caches in Spark and GPU unchanged due to their unified memory managers and impact on execution memory.

Reuse Overhead: To understand the overhead of lineage tracing and cache probing, we explore a hyper-parameter tuning scenario. We execute the core logic of L2SVM with varying input sizes, iteration counts, and percentages of reusable instructions. First, we fix the iteration count at 200 (total 2M instructions) and vary input sizes in [800B, 8MB]. While increasing input sizes scales the compute cost per instruction, the overhead from lineage tracing and cache management remains constant. To simulate reuse, we adjust the fraction of reusable instructions from 20% to 80% by randomly repeating hyperparameters, where the reusable instructions contain primarily binary matrix-vector computations. Figure 11(a) compares Base with different configurations. The *Trace* setting enables only tracing, introducing tracing overhead. *Probe* refers to reuse enabled but with no reusable instructions (i.e., maximum overhead with no reuse benefits). Here, for input sizes smaller than 8MB, the total execution time of Base is dominated by interpretation overhead, as well as variable and statistics management. Lineage tracing and probing further increase this overhead by 1.3x and 2x. For small input data, reuse does

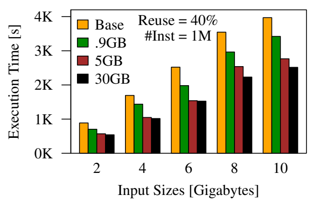


(a) Reuse Overhead - Sizes

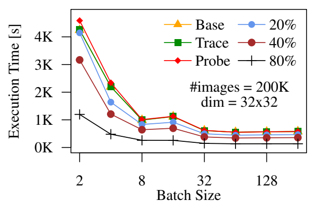


(b) Reuse Overhead - #Instructions

Figure 11: Basic Lineage Tracing and Reuse Overhead.



(a) Cache Size Comparison



(b) Tracing Overhead GPU

Figure 12: Influence of Cache Sizes on Reuse Potential and GPU Backend Tracing Overhead.

not help due to relatively low compute cost. However, for larger inputs (8MB), the tracing and probing overheads become negligible, and the reuse settings show improvements from 1.1x (20% reuse) to 3x (80% reuse). Second, to further study this scenario, we vary the instruction count from 1M to 5M for the fixed 8MB input. Increasing instruction count scales the caching related overheads. Figure 11(b) shows the probing overhead increases with instruction count, reaching 15% for 5M instructions, while the tracing overhead remains moderate. However, already 20% reuse amortizes these overheads by reusing intermediates and applying compaction (see Figure 5), while 40% reuse improves by 1.5x. We further compare a reuse setting of a larger cache with no cache eviction (40%INF). This setting does not yield any further speedup as MEMPHIS's caching policy maintains the objects with high reuse potential even in a small 5GB cache.

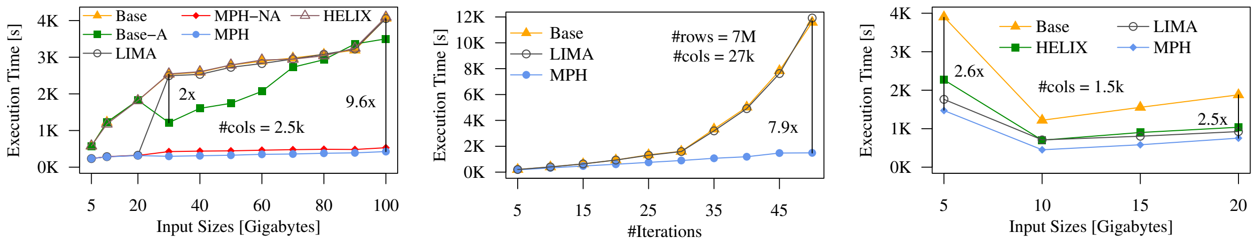
Cache Size Comparison: To evaluate the impact of cache sizes in the driver, we utilize the same experiment for varying input sizes in [2GB, 10GB], (with 1M instructions and 40% reusable), and three cache sizes: 900MB, 5GB, and 30GB. The 8GB and 10GB input matrices are distributed and produce Spark operations. Figure 12(a) shows, that even a 900MB cache consistently achieves 1.2x speedup. For smaller input sizes, 5GB and 30GB show similar speedup, while for larger inputs, the 5GB cache yields slightly less speedup compared to the 30GB cache (1.4x vs. 1.6x). The speedup comes from reusing local intermediates and Spark RDDs and actions (including `prefetch`), even after multiple evictions—proving the robustness of our eviction policies.

GPU Cache Eviction: To evaluate the GPU memory management, we utilize an ensemble convolutional neural network (CNN) scoring of 200K 32×32 images with varying batch sizes and different reuse settings (randomly repeated images identified by pixel-encoded IDs). We use two CNN models with distinct memory allocation patterns: one with two `conv2d` layers (#output channels = 64, 128) and ReLU activations, and the other with three `conv2d` layers (#output channels = 64, 192, 256) and ReLU activations. Both CNNs employ two fully-connected layers with ReLU and Softmax activation after the `conv2d` layers for classification. Figure 12(b) shows that the overhead of probing remains moderate, at 8%, even for a small batch size of 2 (2.6M GPU instructions), and is offset by only 20% reuse. From batch size 4, despite a large number of evictions (255K/139K recycled/reused pointers for batch size 4), reuse settings of 20%, 40%, and 80% yield consistent improvements of 1.3x, 1.6x, and 4x, respectively.

Conclusions: These micro benchmarks show that MEMPHIS's lineage tracing and probing overhead remain relatively low even for a large number of instructions. The robustness optimizations, such as the compaction of lineage DAGs, effectively amortize the probing overhead even when reuse is low. Moreover, the backend-specific eviction policies retain reuse benefits, despite frequent evictions and smaller cache sizes.

Table 3: Overview of ML Pipeline Use Cases & Datasets

Name	Use Case	Dataset	# Rows	# Columns	Influential Techniques
HCV	Grid Search / Cross Validation	Synthetic	[270K, 2.7M]	2.5K	Async. OPs, local & RDD reuse
PNMF	Non-negative Matrix Factorization	MovieLens	7M	27K	Checkpoint placement
HBAND	Hyperband Model Selection	Synthetic	[425K, 1.7M]	1.5K	Multi-level reuse, delayed caching
CLEAN	Data Cleaning Pipelines	APS	[60K, 7.2M]	170	Large #intermediates & #evictions
HDROP	Dropout Rate Tuning	KDD 98	95K	469	Local and GPU ptr. reuse
EN2DE	Machine Translation Inference	WMT1́4	200K	1	Recycle & reuse GPU ptrs.
TLVIS	Transfer Learning Feature Extraction	ImageNet, CIFAR-10	10K images	224 × 224, 32 × 32	Evictions & mem. management



(a) HCV (b) PMNF (c) HBAND

Figure 13: Performance of End-to-end ML Pipelines, part I.

6.3 ML Pipelines Performance

We now describe the performance impact of multi-backend reuse on end-to-end ML pipelines. For a balanced view, we evaluate a diverse set of workloads with different characteristics.

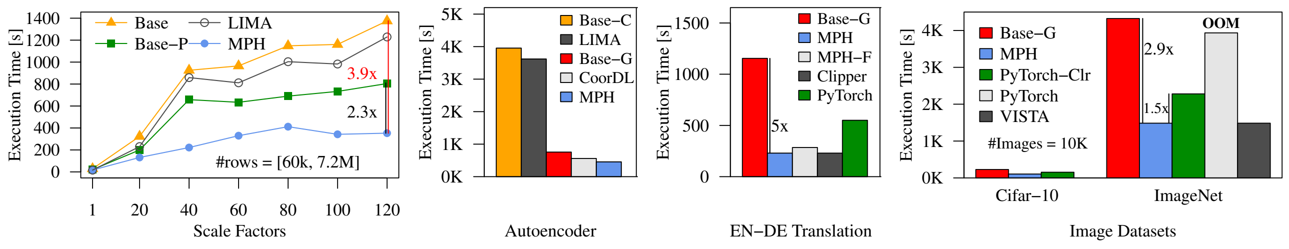
Pipeline Summary: Table 3 provides an overview of the used ML pipelines and datasets. The pipelines include: (1) Grid search hyper-parameter optimization of cross-validated linear regression (HCV); (2) Poisson non-negative matrix factorization (PNMF); (3) model search via Hyperband-like multi-armed bandit [74] and weighted ensemble learning (HBAND); (4) pipeline enumeration for data cleaning [114] (CLEAN) (5) dropout-rate optimization for Autoencoder (HDROP); (6) a pre-trained scoring network for English to German translation (EN2DE); and (7) transfer learning for computer vision models (TLVIS). All pipelines leverage SystemDS's built-in functions, with all compiler and runtime optimizations enabled for MEMPHIS. The *Influential Techniques* column highlights the most impactful optimizations and key workload characteristics for each use case.

Dataset Description: Lineage-based reuse is largely independent of data skew. We combine real and synthetic datasets to evaluate varying data characteristics. MovieLens [54] is a movie rating dataset containing 20M ratings (138K unique users, 27K unique movies). For pre-processing, we integer encode and replicate rows. APS [1] is a classification dataset, collected from components of SCANIA trucks, for classifying Air Pressure System (APS) failures. This dataset has 60K entries and 0.6% missing values. KDD98 is a regression dataset for the return from donation campaigns. We perform recoding on categorical and binning (10 equi-width bins) on numerical features. The WMT2014 dataset [27, 81] for English-to-German translation comprises news and web crawls. We use a 200K-word subset of this dataset. ImageNet [4] and CIFAR-10 [67] are popular image datasets. For pre-processing, we resized the ImageNet images to 224×224×3 and CIFAR-10 images to 32×32×3, then linearized these images.

Cross-Validation: HCV calls a cross-validated linear regression with Example 4.1 at its core, for 10 different regularization parameters. HCV uses R^2 to find the best parameters. We vary the input size in [5 GB, 20 GB] and compare Base, LIMA, HELIX, and MEMPHIS, where Base-A and MPH are with and Base and MPH-NA are without the asynchronous operators. Figure 13(a) shows MPH is 9.6x faster than Base by reusing $\mathbf{X}^\top\mathbf{X}$ and $\mathbf{X}^\top\mathbf{y}$ for each fold and executing concurrent jobs through `prefetch`. Although, MPH uses 2x more cluster memory compared to Base for storing the cached RDDs, the extra memory usage does not impact the execution performance. Starting from 25 GB input size, $\mathbf{X}^\top\mathbf{X}$ and $\mathbf{X}^\top\mathbf{y}$ are placed in Spark. LIMA reuses only local intermediates up to 20 GB, whereas MPH reuses in all settings. HELIX performs similar to Base as HCV has no coarse-grained reuse opportunities (i.e., no repeating top-level ML tasks). Base-A yields 2x speedup due to concurrent execution, but the speedup decreases for larger inputs (#partitions > #cores). MPH is 20% faster than MPH-NA due to parallel operator execution.

Matrix Factorization: Poisson Non-negative Matrix Factorization (PNMF) [79] factorizes a matrix $\mathbf{X}$ into factors $\mathbf{W}$ and $\mathbf{H}$ such that $\mathbf{X} \approx \mathbf{WH}$. PNMF iteratively updates $\mathbf{W}$ and $\mathbf{H}$ via its update rules. For PNMF on the MovieLens dataset with rank 100, $\mathbf{W}$ (7M × 100) becomes distributed—as shown in Figure 9(c)—while $\mathbf{H}$ (100 × 27K) remains local. We vary the number of iterations to study the performance impact of the compiler-placed checkpoints (`persist`). Figure 13(b) shows that, as the iteration count exceeds 30, Base and LIMA significantly slow down due to the increasing size of the Spark jobs re-executing all previous iterations. However, MPH yields a 7.9x speedup (with 4x more memory usage) by persisting $\mathbf{W}$ in each iteration (see Section 5.2).

Model Search: HBAND has two phases. We first utilize successive halving to fine-tune the hyper-parameters of L2SVM and multi-class logistic regression (MLRG). The inner loop performs a grid search over regularization parameters (`reg`) and intercept options (0, 1, or 2), while the outer loop iterates through five brackets, each halving the `reg` list (starting with 25 values) and doubling the iteration count (starting from 10). We then apply weighted ensemble learning to combine the best L2SVM and MLRG models. The ensemble weights are optimized via a random search over 1K weight configurations. Figure 13(c) shows the results for varying data sizes. MPH yields 2.6x/2.5x speedups for 5 GB/20 GB inputs over Base by reusing the previous iterations of successive halving and the **XB** multiplication in weighted class probability computations. Reused objects include many RDDs (≈ 4K), Spark actions (≈ 2K), and local matrices (≈ 40K). Our compiler enabled *delayed caching* for RDDs for MPH. MEMPHIS



(a) CLEAN (b) HDROP (c) EN2DE (d) TLVIS

Figure 14: Performance of End-to-end ML Pipelines, part II.

is 40% faster than HELIX (reuses **XB** operators) and LIMA. Even for local operations (5 GB), MPH is 20% faster than LIMA.

Data Cleaning: CLEAN enumerates data cleaning pipelines, leveraging the downstream ML algorithm for feedback. We construct 12 pipelines combining primitives for missing value imputation (`imputeByMean`, `imputeByMode`), outlier detection (`outlierByIQR`), normalization (`standard scaling`, `min-max`), class imbalance (`underSampling`), and dimensionality reduction (PCA) for a downstream L2SVM task and return the top-3 pipelines. The order of the primitives in each pipeline is data-dependent, (e.g., imputation and outlier removal before normalization). These pipelines can be auto-generated using AutoML [114]. We vary the data size [60K, 7.2M] using a scale factor, which utilizes row append to replicate the input data, and compare Base, Base with parallel feature processing using multi-threading [23] (Base-P), and MEMPHIS. Figure 14(a) shows, for scale factor 120, MPH yields 3.9x/3.5x/2.3x speedups over Base/LIMA/Base-P by reusing the repeating primitives. Most cleaning primitives operate feature-wise, producing many intermediates, which leads to repeated cache spills. However, our cache eviction logic continues to reuse the local and Spark operator outputs.

Dropout-Rate Tuning: HDROP tunes the dropout rate from 5% to 50% of an Autoencoder (AE) using grid search. The AE has two hidden layers of sizes 500 and 2 and a dropout layer. For each dropout rate, we train the AE for 10 epochs with batch size 256. We construct an input data pipeline (IDP) with normalization and a feature transformation map of binning, recoding, one-hot encoding, and apply this pipeline batch-wise in every iteration. Figure 14(b) shows the results of comparing Base with CPU instructions (Base-C), Base with CPU and GPU instructions (Base-G), LIMA, CoorDL, and MEMPHIS on the KDD98 dataset. Although HDROP has modest reuse opportunities, MPH achieves 1.7x speedup over Base-G by reusing the batch-wise IDP across epochs. The feature transformation is reused on the host, while the normalization is reused on the GPU. CoorDL, as a representative of IDP reuse frameworks, only reuses the CPU component of the IDP and is 24% slower than MPH. This experiment is another example of efficient fine-grained reuse across multiple backends.

Language Translation: The EN2DE pipeline comprises GPU scoring with a pre-trained language translation model, and exhibits fine-grained prediction caching potential [33]. We use pre-trained word embeddings for English and German and their dictionaries, along with a pre-trained model, comprising four fully-connected layers with ReLU and Softmax for translation. The word embeddings for both English and German are trained on Wikipedia and 300-dimensional. The input is a 200K-word sequence of news content. Figure 14(c) compares Base with GPU instructions (Base-G), operator-at-a-time reuse (MPH-F), which disables multi-level reuse (see Section 3.3), Clipper, and MEMPHIS. MPH yields a 5x speedup over Base-G by reusing scoring results at the host—completely eliminating GPU computations for the reused words. In contrast, MPH-F reuses GPU pointers for the reusable instructions, yielding a 4x speedup, despite frequent evictions including 325K recycled pointers. Clipper performs similar to MPH by reusing the predictions at the host.

Transfer Learning: Transfer learning is a widely used alternative to training large models from scratch. Practitioners often evaluate different pre-trained models to identify the most suitable model-layer pair for the downstream task and input dataset [93, 104]. TLVIS utilizes three pre-trained CNN models: AlexNet [68], VGG16 [115], and ResNet18 [57], and extracts the following layers (by applying the pre-trained weights on the test images) for transfer learning: `Conv2d` of layer4 (Conv4) to fully-connected layer7 (FC7) from AlexNet, Conv5 to FC7 layers from VGG and the last four residual blocks from ResNet. The pre-trained layers are frozen during feature extraction, and a proxy of a linear classifier is used to rank the extracted features [95, 119]. We split the CIFAR-10 and ImageNet datasets into non-overlapping training and test sets, with 10K images in each test set, and we execute the pipelines in the GPU. Figure 14(d) shows that MEMPHIS yields 2x and 3x speedups for CIFAR-10 and ImageNet test sets by reusing the intermediates during repetitive feature extractions. MEMPHIS compiles an `evict(100)` instruction between models (*eviction injection*) to free up the allocated pointers, and the GPU memory manager efficiently recycles the intermediates without compromising the reuse benefits. For instance, 30K and 17.5K pointers are reused and recycled for ImageNet, respectively. VISTA, as a specialized system for transfer learning, performs similar to MPH by applying CSE across pipelines.

Comparison with PyTorch: For comparison with another ML system, we compare MEMPHIS with PyTorch for EN2DE and TLVIS. All intermediates are represented as `torch` tensors. For TLVIS, we utilize PyTorch's pre-trained models and API to freeze layers. Additionally, we transfer the model parameters and datasets to the GPU before starting the mini-batch processing to enable PyTorch's compiler optimizations and speculative GPU memory management [76]. PyTorch with `torch.compile` (PyTorch) fails with out-of-memory and requires manual cleanups of the allocation cache (`empty_cache()`) after each model [31, 32] (PyTorch-Clr). Figures 14(c) and 14(d) show that PyTorch—as a specialized system for DNN training—is 2x/1.9x faster than Base-G for EN2DE and TLVIS. However, PyTorch fails to reuse predictions and repeated feature extractions and is 2.4x and 1.5x slower than MPH for EN2DE and TLVIS, respectively.

Conclusion: Overall, our workload-aware compiler-assisted reuse, optimizations, inter-backend parallelism, and memory management show competitive performance compared to other systems, which include ML systems as well as specialized application-specific reuse frameworks, demonstrating our framework's effectiveness in a broader range of scenarios.

7 RELATED WORK

Our compiler-assisted, multi-backend reuse in ML systems is related to the reuse of ML and query intermediates, RDD caching, GPU memory management, and operator scheduling.

Reuse of ML Pipeline Intermediates: Prior work has recognized significant reuse opportunities in exploratory data science workflows. Columbus [130] and KeystoneML [116] automatically materialize and reuse selected intermediates within and across ML pipelines. Subsequent work—including Alpine Meadow [112], HELIX [125], collaborative optimizer [39], HYPPO [66] and, result sharing for what-if analysis [51]—apply CSE and cost-based materialization for reusing ML task results such as data preparation, feature engineering, and model training. Other work focuses on reuse within specific workloads: tf.Data [92], Cachew [53], CoorDL [88], and TensorSocket [105] reuse pre-processed mini-batches in DNN training; Clipper [33] and PRETZEL [73] apply CSE and caching to predictions; MISTIQUE [123] enables caching and querying model intermediates; as well as OneAccess [65], Ease.ml [77], and SystemDS federated [19] enable multi-tenant resource sharing in ML clusters. Most of these systems only support coarse-grained reuse (of top-level primitives) and apply reuse in an isolated manner (independent of multiple backends, operator scheduling, and memory management).

Reuse of Query Intermediates: Our work on reuse is inspired by the extensive research on reusing query intermediates in database systems. Reuse is used for various aspects including buffer pool page caching in CPU/GPU memory [82], scan sharing [13, 121], request batching [72], subexpression reuse [63], materialized views [6, 63], as well as multi-query optimization [107]. Work on recycling intermediates in MonetDB [60], transient materialized views [135], and Firebolt [9] reuse previously materialized in-memory or spool intermediates. CoGaDB [28] leverages a similar reuse of GPU intermediates, exploiting data locality. In contrast to this line of work, MEMPHIS provides holistic multi-backend reuse for linear algebra programs.

RDD Caching and Reuse: Prior work on RDD caching largely falls into three categories. First, heuristics-based caching utilizes known data dependencies to select intermediates for caching. SystemML [24] injects `persist()` directives after persistent reads (text to binary) and before loops for read-only variables. Emma [10] caches RDDs that are referenced multiple times. Second, DAG-aware eviction policies such as Least Reference Count (LRC) [127, 128], and Most Reference Distance (MRD) [99] extend Spark's default LRU to prioritize frequently-used RDDs. LRC monitors the number of consumers for each RDD and evicts partitions of those with the least active consumers. MRD considers both the number and distance (number of stages) of consumers, evicting RDDs with fewer active consumers farther away in the DAG. Third, caching frameworks such as Juggler [8], Agile-Ant [7], and MEMTUNE [126] optimize distributed caching decisions in a cost-based manner by analyzing data dependencies and access patterns for individual Spark jobs. In contrast, MEMPHIS identifies fine-grained redundancy at runtime and reuses RDDs across jobs and conditional control flow programs.

GPU Memory Management: GPUs are widely used for DNN workloads and many specialized techniques for GPU memory management exist. GPU memory is a limiting factor in DNN design [50, 57, 68], and many DNN job failures are caused by running out of GPU memory due to large batch sizes, skewed memory usage across layers, memory fragmentation, and mispredicting intermediate sizes [131]. TensorFlow [118] and JAX [14] preallocate nearly all GPU memory to avoid memory fragmentation and frequent calls to `cudaMalloc` and `cudaFree`. PyTorch [132] uses a pool allocator [71], which recycles free memory pointers. Prior work [29, 61, 111, 133] on materialization also discards activations in the forward pass to reduce memory pressure and recomputes them during the backward pass. Further, asynchronous swapping [58, 84, 98] allows offloading activations from GPU memory to host, freeing up memory for ongoing computations and re-loading them on demand. Another line of work proposes more accurate estimators for the size of intermediates [46, 110]. These techniques are designed for single DNN training and are independent of reusing intermediates in ML pipelines with multiple training and inference tasks.

Operator Scheduling: The performance impact of operator scheduling has been investigated before. GPipe [59] and DAPPLE [44] explore pipeline parallelism across mini-batches, and partition the operators to increase parallelism and remove pipeline bubbles (overlapping computation and communication). PipeDream [94] extends this work for asynchronous convergence by scheduling the mini-batches based on a brief GPU profiling and multiple versions of weights. Alpa [134] combines data and model parallelism for large DNNs by automatically compiling cost-optimal plans for data and model parallelism. CoCoNet [62] introduced a domain-specific language for specifying combinations of computation and communication, along with a compiler that generates optimized custom kernels. Additionally, NVIDIA offers higher-level programming abstractions [41] and a unified memory manager including pre-fetching capabilities [56]. In contrast, MEMPHIS's operator ordering and asynchronous operators exploit parallelism across multiple backends, integrate lineage-based reuse, and handle data-centric ML pipelines ranging from pre-processing to training.

8 CONCLUSIONS

To summarize, we introduced MEMPHIS as a holistic framework for efficient, multi-backend reuse of intermediates and memory management in ML systems. Our hierarchical lineage cache seamlessly allows reuse across heterogeneous backends. We devised tailor-made eviction policies for Spark and GPUs, along with related memory management techniques. Our compiler extensions improve reuse potential, reduce runtime overheads, and enable concurrent execution. Our experiments have shown robust improvements across diverse workloads. In conclusion, the increasing complexity of ML pipelines, coupled with diverse data modalities and heterogeneous backends, inevitably introduces redundancy across different backends. This growing complexity and heterogeneity poses challenges for library developers and users, as manual redundancy elimination becomes infeasible. Our compiler-assisted, runtime-based multi-backend lineage cache effectively addresses these challenges. The underlying concepts and optimization techniques are broadly applicable in modern ML systems. Interesting future work includes (1) exploring cost-based operator scheduling for reuse-aware operator placement, (2) query processing over lineage traces for model debugging, and (3) extending lineage tracing for fairness constraints [52].

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